PRESS RELEASE

Source: Tokyo Institute of Technology, Center for Public Affairs and Communications

For immediate release: 6 December 2016
Tokyo Institute of Technology research: 3D solutions to energy savings in silicon power transistors

(Tokyo, 6 December) **Tokyo Tech researchers demonstrate operation energy-savings in a low price silicon power transistor structure by scaling down in all three dimensions.**

In electronics, lower power consumption leads to operation cost savings, environmental benefits and the convenience advantages from longer running devices. While progress in energy efficiencies has been reported with alternative materials such as SiC and GaN, energy-savings in the standard inexpensive and widely used silicon devices are still keenly sought. K Tsutsui at Tokyo Institute of Technology and colleagues in Japan have now shown that by scaling down size parameters in all three dimensions their device they can achieve significant energy savings.

Tsutsui and colleagues studied silicon insulated gate bipolar transistors (IGBTs), a fast-operating switch that features in a number of every day appliances. While the efficiency of IGBTs is good, reducing the ON resistance, or the voltage from collector to emitter required for saturation ($V_{ce(sat)}$), could help increase the energy efficiency of these devices further.

Previous investigations have highlighted that increases in the "injection enhancement (IE) effect", which give rise to more charge carriers, leads to a reduction in $V_{ce(sat).}$ Although this has been achieved by reducing the mesa width in the device structure, the mesa resistance was thereby increased as well. Reducing the mesa height could help counter the increased resistance but is prone to impeding the (IE) effect. Instead the researchers reduced the mesa width, gate length, and the oxide thickness in the MOSFET to increase the IE effect and so reduce $V_{ce(sat)}$ from 1.70 to 1.26 V. With these alterations the researchers also used a reduced gate voltage, which has advantages for CMOS integration.

They conclude, "It was experimentally confirmed for the first time that significant $V_{ce(sat)}$ reduction can be achieved by scaling the IGBT both in the lateral and vertical dimensions with a decrease in the gate voltage."

Background

Insulated gate bipolar transistors (IGBTs)

These are three terminal devices used as switches or rectifiers. With simple gate-drive characteristics and high-current and low-saturation-voltage capabilities they combine the benefits of two other types of transistors - metal-oxide-semiconductor field effect transistors (MOSFETs) and bipolar transistors.

3D scaling of IGBTs

The researchers reduced the mesa width, gate length, and the oxide thickness in the MOSFET by a factor of $1/k$, and compared devices with values of 1 and 3 for k. Because the fabrication of narrow mesas can cause problems they also reduced the trench depth by $1/k$. Although this has a slightly negative effect on the IE effect, it has considerable benefits for fabrication ease and cost and the dependence of ($V_{ce(sat)}$) on the trench depth was deemed to be small. The gate voltage was also decreased by a factor of $1/k$, while the cell pitch was maintained at 16 µm.

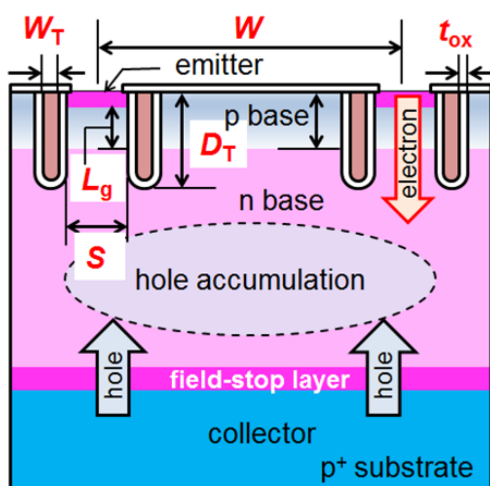
Reference

K. Kakushima[1], T. Hoshii[1], K. Tsutsui[1], A. Nakajima[2], S. Nishizawa[2], H. Wakabayashi[1], I. Muneta[1], K. Sato[3], T. Matsudai[4], W. Saito[4], T. Saraya[5], K. Itou[5], M. Fukui[5], S. Suzuki[5], M. Kobayashi[5], T. Takakura[5], T. Hiramoto[5], A. Ogura[6], Y. Numasawa[6], I. Omura[7], H. Ohashi[1], and H. Iwai[1], Experimental verification of a 3D scaling principle for low $V_{ce(sat)}$ IGBT, Technical Digest of IEDM2016, Session 10.6, (2016), http://ieee-iedm.org/

1. Tokyo Inst. of Technology, Yokohama, Japan
2. Nat. Inst. Advanced Industrial Science and Technology, Tsukuba, Japan
3. Mitusbishi Electric, Fukuoka, Japan
4. Toshiba Corp., Tokyo, Japan
5. The University of Tokyo, Tokyo, Japan
6. Meiji University, Kawasaki, Japan
7. Kyushu Inst. of Technology, Kitakyushu, Japan

*corresponding author e-mail ktsutsui@ep.titech.ac.jp

Figure.



Caption

Trench gate IGBT schematic indicating the mesa width (*S*), gate length (L_g), and the oxide thickness in the MOSFET (t_{ox}), cell pitch (*W*), and the trench depth (D_T).

Contact

Emiko Kawaguchi
Center for Public Affairs and Communications,
Tokyo Institute of Technology
E-mail.media@jim.titech.ac.jp
+81-3-5734-2975

About Tokyo Institute of Technology

Tokyo Institute of Technology stands at the forefront of research and higher education as the leading university for science and technology in Japan. Tokyo Tech researchers excel in a variety of fields, such as material science, biology, computer science and physics. Founded in 1881, Tokyo Tech has grown to host 10,000 undergraduate and graduate students who become principled leaders of their fields and some of the most sought-after scientists and engineers at top companies. Embodying the Japanese philosophy of “monotsukuri,” meaning technical ingenuity and innovation, the Tokyo Tech community strives to make significant contributions to society through high-impact research.
Website: http://www.titech.ac.jp/english/